AMENDMENTS TO THE SPECIFICATION

In the specification

Please amend paragraph **[0027]** as follows:

[0027] Another input to the model is a deposition bias associated with the layers of material deposited on the wafer. The deposition bias indicates the variation between the actual deposition profile "as deposited" and the predicted deposition profile "as drawn." For example, the pattern density "as deposited" (i.e., the pattern density that actually results on the chip may not necessarily reflect the pattern density "as drawn" (i.e., the pattern density as intended in the design of the chip). This is due, in part, to the fact that during the IC processing steps, the film (either metal or insulating dielectrics) transfer the pattern in different ways depending on the deposition process used (e.g., electroplated, thermal chemical vapor ~~depsotion~~ deposition – ~~CVS~~ CVD, physical vapor deposition – PVD, plasma enhanced (PE), atmospheric (AP) or low pressure (LP) or subatmospheric (SA) chemical vapor deposition – PECVD, APCVD, LPCVD, SACVD, spin coating, atomic layer deposition – ~~AVD~~ ALD, and the like). Each of these processing methods can affect the underlaying pattern density differently. For example, PECVD deposited films have a negative bias compared to SACVD deposited films. Furthermore, the types of film (fluorine doped silicate glass, FSG, compared to undoped silicate glass USG or SiO2) have different effects on the pattern density. As depicted in Figs. 4A and 4B, SiO2 or USG films can have a positive bias 402, while FSG films have a negative bias 404.